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PTO/SB/05 (4/98)

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UTILITY
PATENT APPLICATION
TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. MI22-1171

First Inventor or Application Identifier Salman Akram

Title Methods of Forming a Transistor Gate

Express Mail Label No. EL369520905US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

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- 1.
- ☒
- * Fee Transmittal Form (e.g., PTO/SB/17)
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- 2.
- ☒
- Specification [Total Pages 27] 1
-
- (preferred arrangement set forth below) Inc. Title Pg.

- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

- 3.
- ☒
- Drawing(s) (35 U.S.C. 113) [Total Sheets 4] 1

4. Oath or Declaration [Total Pages 3] 1

a. ☐ Newly executed (original or copy)b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)

- i.
- ☐
- DELETION OF INVENTOR(S)
-
- Signed statement attached deleting
-
- inventor(s) named in the prior application,
-
- see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY
FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT
IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

- 5.
- ☐
- Microfiche Computer Program (Appendix)

6. Nucleotide and/or Amino Acid Sequence Submission
-
- (if applicable, all necessary)

- a. ☐ Computer Readable Copy
- b. ☐ Paper Copy (identical to computer copy)
- c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

- 7.
- ☐
- Assignment Papers (cover sheet & document(s))

- 8.
- ☐
- 37 C.F.R. § 3.73(b) Statement
- ☐
- Power of
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- (when there is an assignee)
- ☐
- Attorney

- 9.
- ☐
- English Translation Document (if applicable)

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- Statement (IDS)/PTO-1449
- ☐
- Citations

- 11.
- ☒
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16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No. 08 / 993,663

Prior application information: Examiner S. Mulpuri Group / Art Unit: 2812

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Signature		Date	April 14, 1999

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EL 369520905

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/993,663
Priority Filing Date December 18, 1997
Inventor Salman Akram et al.
Assignee Micron Technology, Inc.
Priority Group Art Unit 2812
Priority Examiner S. Mulpuri
Attorney's Docket No. MI22-1171
Title: Methods of Forming a Transistor Gate (As Amended)

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: James D. Shaurette (Tel. 509-624-4276; Fax 509-838-3424)
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AMENDMENTS

In the Title

Please replace the title with --Methods of Forming a Transistor
Gate--.

In the Specification

At p. 1, before the "Technical Field" section, insert

1 **--RELATED PATENT DATA**

2 This patent application is a continuation resulting from U.S. Patent
3 Application Serial No. 08/993,663, which was an application filed on
4 December 18, 1997.--

5
6 **In the Claims**

7 Cancel claims 1-50.

8 Add the following new claims 51-75.

9
10 51. A method of forming a transistor gate comprising:
11 forming a gate oxide layer over a semiconductive substrate;
12 providing at least one of fluorine or chlorine within the gate oxide
13 layer; and
14 forming a gate proximate the gate oxide layer after the providing.

15
16 52. The method of claim 51 wherein the chlorine is provided in
17 the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm³
18 to about 1×10^{21} atoms/cm³.
19
20
21
22
23

53. The method of claim 51 wherein the gate comprises opposing lateral edges and a central region therebetween, the chlorine being provided within the gate oxide layer to a greater concentration proximate at least one of the gate edges than in the central region.

54. The method of claim 51 wherein the providing comprises providing fluorine.

55. A method of forming a transistor gate comprising:
forming a gate and a gate oxide layer in overlapping relation, the gate having opposing edges and a center therebetween, the gate oxide having a center and outwardly exposed opposing edges laterally aligned with the edges of the gate; and
concentrating at least one of chlorine or fluorine in the gate oxide layer within the overlap more proximate at least one of the outwardly exposed oxide gate edges than the center.

56. The method of claim 55 wherein the concentrating comprises concentrating fluorine.

1 57. The method of claim 55 wherein the gate is formed to have
2 a gate width between the edges of 0.25 micron or less, the concentrating
3 forming at least one concentration region in the gate oxide which
4 extends laterally inward from the at least one gate edge no more than
5 about 500 Angstroms.

6
7 58. The method of claim 55 wherein the concentrating comprises
8 diffusion doping.

9
10 59. The method of claim 55 wherein the concentrating comprises
11 ion implanting.

12
13 60. The method of claim 55 wherein the removing comprises
14 removing portions of the gate oxide layer not overlapping the gate.

15
16 61. The method of claim 55 wherein the concentrating follows
17 the removing.

62. A method of forming a transistor gate comprising:
forming a gate and a gate oxide layer in overlapping relation, the
gate having opposing edges and a central region therebetween;
forming sidewall spacers comprising at least one of the chlorine or
fluorine proximate the opposing edges; and
doping the gate oxide layer within the overlap with at least one
of chlorine or fluorine proximate the opposing gate edges and leaving
the central region substantially undoped with chlorine and fluorine.

63. The method of claim 62 wherein the doping provides a
dopant concentration in the gate oxide layer proximate the edges from
about 1×10^{19} atoms/cm³ to about 1×10^{21} atoms/cm³.

64. The method of claim 62 further comprising removing portions
of the gate oxide layer not overlapping the gate.

65. The method of claim 62 wherein the doping comprises
diffusion doping at least one of chlorine or fluorine from the spacers
into the gate oxide layer.

66. The method of claim 65 further comprising annealing the
spacers to provide the diffusion doping.

67. The method of claim 62 wherein the doping comprises doping with fluorine.

68. A method of forming a transistor gate comprising the following sequential steps:

forming a gate over a gate oxide layer, the gate having opposing lateral edges;

forming sidewall spacers comprising at least one of chlorine or fluorine proximate the opposing lateral edges; and

diffusion doping at least one of chlorine or fluorine into the gate oxide layer beneath the gate from laterally outward of the gate edges.

69. The method of claim 68 wherein the doping provides a dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm³ to about 1×10^{21} atoms/cm³.

70. The method of claim 68 wherein the doping provides a pair of spaced and opposed concentration regions in the gate oxide which extend laterally inward from the gate edges no more than about 500 Angstroms.

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1 71. The method of claim 68 wherein the doping provides a pair
2 of spaced and opposed concentration regions in the gate oxide which
3 extend laterally inward from the gate edges no more than about
4 500 Angstroms, the concentration regions having an average dopant
5 concentration in the gate oxide layer proximate the edges from about 1×10^{19}
6 atoms/cm^3 to about $1 \times 10^{21} \text{ atoms/cm}^3$.

8 72. The method of claim 71 wherein the gate oxide layer
9 between the concentration regions is substantially undoped with chlorine
10 and fluorine.

11
12 73. The method of claim 68 further comprising removing portions
13 of the gate oxide layer not beneath the gate.

14
15 74. The method of claim 68 wherein the diffusion doping
16 comprises annealing the sidewall spacers.


17
18 75. The method of claim 68 wherein the diffusion doping
19 comprises diffusion doping fluorine.
20
21
22
23

REMARKS

Claims 1-50 are canceled, and new claims 51-75 are added.
Claims 51-75 are pending in the application, and Applicant requests
examination of such pending claims.

Respectfully submitted,

Dated: Apr. 14, 1999

By: 
James D. Shaurette
Reg. No.: 39,833

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

**Semiconductor Processing Method And Field Effect
Transistor**

* * * * *

INVENTOR

**Salman Akram
Akram Ditali**

ATTORNEY'S DOCKET NO. MI22-695

65443232660

SEMICONDUCTOR PROCESSING METHOD AND FIELD EFFECT TRANSISTOR

TECHNICAL FIELD

This invention relates to methods of forming transistor gates and to transistor constructions.

BACKGROUND OF THE INVENTION

As transistor gate dimensions are reduced and the supply voltage remains constant, the lateral field generated in MOS devices increases. As the electric field becomes strong enough, it gives rise to so-called "hot-carrier" effects in MOS devices. This has become a significant problem in NMOS devices with channel lengths smaller than 1.5 micron, and in PMOS devices with sub-micron channel lengths.

High electric fields cause the electrons in the channel to gain kinetic energy, with their energy distribution being shifted to a much higher value than that of electrons which are in thermal equilibrium within the lattice. The maximum electric field in a MOSFET device occurs near the drain during saturated operation, with the hot electrons thereby becoming hot near the drain edge of the channel. Such hot electrons can cause adverse effects in the device.

First, those electrons that acquire greater than or equal to 1.5 eV of energy can lose it via impact ionization, which generates electron-hole pairs. The total number of electron-hole pairs generated by impact

ionization is exponentially dependent on the reciprocal of the electric field. In the extreme, this electron-hole pair generation can lead to a form of avalanche breakdown. Second, the hot holes and electrons can overcome the potential energy barrier between the silicon and the silicon dioxide, thereby causing hot carriers to become injected into the gate oxide. Each of these events brings about its own set of repercussions.

Device performance degradation from hot electron effects have been in the past reduced by a number of techniques. One technique is to reduce the voltage applied to the device, and thus decrease in the electric field. Further, the time the device is under the voltage stress can be shortened, for example, by using a lower duty cycle and clocked logic. Further, the density of trapping sites in the gate oxide can be reduced through the use of special processing techniques. Also, the use of lightly doped drains and other drain engineering design techniques can be utilized.

Further, it has been recognized that fluorine-based oxides can improve hot-carrier immunity by lifetime orders of magnitude. This improvement is understood to mainly be due to the presence of fluorine at the Si/SiO₂ interface reducing the number of strained Si/O bonds, as fewer sites are available for defect formation. Improvements at the Si/SiO₂ interface reduces junction leakage, charge trapping and interface trap generation. However, optimizing the process can be complicated. In addition, electron-trapping and poor leakage characteristics can make

such fluorine-doped oxides undesirable and provide a degree of unpredictability in device operation. Use of fluorine across the entire channel length has been reported in, a) K. Ohyu et al., "Improvement of SiO₂/Si Interface Properties by Fluorine Implantation"; and b) P.J. Wright, et al., "The Effect of Fluorine On Gate Dielectric Properties".

SUMMARY OF THE INVENTION

In one implementation, a method of forming a transistor includes forming a gate oxide layer over a semiconductive substrate. Chlorine is provided within the gate oxide layer. A gate is formed proximate the gate oxide layer. In another aspect, a gate and a gate oxide layer are formed in overlapping relation, with the gate having opposing edges and a center therebetween. At least one of chlorine or fluorine is concentrated in the gate oxide layer within the overlap more proximate at least one of the gate edges than the center. The center is preferably substantially void of either fluorine or chlorine. In one implementation, at least one of chlorine or fluorine is angle ion implanted to beneath the edges of the gate. In another, sidewall spacers are formed proximate the opposing lateral edges, with the sidewall spacers comprising at least one of chlorine or fluorine. The spacers are annealed at a temperature and for a time period effective to diffuse the fluorine or chlorine from the spacers into the gate oxide

1 layer to beneath the gate. Transistors fabricated by such methods, and
2 other methods, are also contemplated.

3 4 5 **BRIEF DESCRIPTION OF THE DRAWINGS**

6 Preferred embodiments of the invention are described below with
7 reference to the following accompanying drawings.

8 Fig. 1 is a sectional view of a semiconductor wafer fragment in
9 accordance with the invention.

10 Fig. 2 is a sectional view of an alternate semiconductor wafer
11 fragment at one step of a method in accordance with the invention.

12 Fig. 3 is a view of the Fig. 2 wafer at a processing step
13 subsequent to that shown by Fig. 2.

14 Fig. 4 is a sectional view of another semiconductor wafer fragment
15 at an alternate processing step in accordance with the invention.

16 Fig. 5 is a view of the Fig. 4 wafer fragment at a processing
17 step subsequent to that depicted by Fig. 4.

18 Fig. 6 is a view of the Fig. 4 wafer fragment at a processing
19 step subsequent to that depicted by Fig. 5.

20 Fig. 7 is a view of the Fig. 4 wafer at an alternate processing
21 step to that depicted by Fig. 6.

22 Fig. 8 is a sectional view of another semiconductor wafer fragment
23 at another processing step in accordance with the invention.
24

1 Fig. 9 is a view of the Fig. 8 wafer at a processing step
2 subsequent to that depicted by Fig. 8.

3 Fig. 10 is a sectional view of still another embodiment wafer
4 fragment at a processing step in accordance with another aspect of the
5 invention.

6 7 8 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

9 This disclosure of the invention is submitted in furtherance of the
10 constitutional purposes of the U.S. Patent Laws "to promote the
11 progress of science and useful arts" (Article 1, Section 8).

12 A semiconductor wafer fragment in process is indicated in Fig. 1
13 with reference numeral 10. Such comprises a bulk semiconductive
14 substrate 12 which supports field oxide regions 14 and a gate oxide
15 layer 16. In the context of this document, the term "semiconductive
16 substrate" is defined to mean any construction comprising semiconductive
17 material, including, but not limited to, bulk semiconductive materials
18 such as a semiconductive wafer (either alone or in assemblies comprising
19 other materials thereon), and semiconductive material layers (either alone
20 or in assemblies comprising other materials). The term "substrate"
21 refers to any supporting structure, including, but not limited to, the
22 semiconductive substrates described above.

23 A gate structure 18 is formed proximate gate oxide 16, such as
24 in an overlapping relationship. A top gated construction is shown,

1 although bottom gated constructions could also be utilized. Gate
2 construction 18 is comprised of a first conductive material portion 20
3 (i.e., conductively doped polysilicon), and a higher conductive layer 22
4 (i.e., a silicide such as WSi_x). An insulating cap 24 is provided over
5 layer 22, with SiO_2 and Si_3N_4 being example materials. For purposes
6 of the continuing discussion, gate construction 18 defines opposing gate
7 edges 26 and 28, and a center 30 therebetween. The invention is
8 believed to have its greatest impact where the gate width between
9 edges 26 and 28 (i.e., the channel length) is 0.25 micron or less.

10 Chlorine is provided within gate oxide layer 16 as indicated in the
11 figure by the hash marks, and thus between semiconductive material of
12 substrate 12 and transistor gate 18. Chlorine can be provided before
13 or after formation of gate construction 18. For example, the chlorine
14 in layer 16 can be provided by gas diffusion, ion implantation or *in situ*
15 as initially deposited or formed. Preferred dopant concentration of the
16 chlorine within oxide layer 16 is from about 1×10^{19} atoms/cm³ to
17 about 1×10^{21} atoms/cm³. A source, a drain, and insulating sidewall
18 spacers over gate construction 18 can be provided. Chlorine based gate
19 oxides can improve hot-carrier immunity. The chlorine present at the
20 Si/SiO₂ interface reduces the number of strained Si/O bonds, as fewer
21 sites are available for defect formation. Improvements at the Si/SiO₂
22 interface will reduce junction leakage, the probability of charge trapping
23 and interface state generation, thus improving device characteristics.
24

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1 A second embodiment is described with reference to Figs. 2
2 and 3. Like numerals from the first described embodiment are utilized
3 when appropriate, with differences being indicated by the suffix "b" or
4 with different numerals. Wafer fragment 10b ideally comprises a gate
5 oxide layer 16b which is initially provided to be essentially undoped with
6 chlorine. The Fig. 2 construction is subjected to angle ion implanting
7 (depicted with arrows 32) to implant at least one of chlorine or
8 fluorine into gate oxide layer 16b beneath edges 26 and 28 of gate 18.
9 A preferred angle for the implant is between from about 0.5° to about
10 10° from perpendicular to gate oxide layer 16b. An example energy
11 range is from 20 to 50 keV, with 50 keV being a preferred example.
12 An example implant species is SiF_3 , to provide a fluorine dose of from
13 about 1×10^{15} atoms/cm² to about 3×10^{15} atoms/cm², with 2×10^{15}
14 atoms/cm² being a specific example. The resultant preferred implanted
15 dopant concentration within layer 16b is from about 1×10^{19} atom/cm³
16 to about 1×10^{21} atoms/cm³.

17 The concentrated regions from such preferred processing will
18 extend inwardly within gate oxide layer 16b relative to gate edges 26
19 and 28 a preferred distance of from about 50 Angstroms to about
20 500 Angstroms. Such is exemplified in the Figures by boundaries 34.
21 In the physical product, such boundaries would not physically exist, but
22 rather the implant concentration would preferably appreciably drop off
23 over a very short distance of the channel length.
24

Annealing is preferably subsequently conducted to repair damage to the gate oxide layer caused by the ion implantation. Example conditions include exposure of the substrate to a temperature of from 700°C to 1000°C in an inert atmosphere such as N₂ at a pressure from 100 mTorr - 760 Torr for from about 20 minutes to 1 hour. Such can be conducted as a dedicated anneal, or in conjunction with other wafer processing whereby such conditions are provided. Such will also have the effect of causing encroachment or diffusion of the implanted atoms to provide barriers 34 to extend inwardly from edges 26 and 28 approximately from about 50 Angstroms to about 500 Angstroms.

Such provides but one example of doping and concentrating at least one of chlorine or fluorine in the gate oxide layer within the overlap region between the semiconductive material and the gate more proximate the gate edges 26 and 28 than gate center 30. Such preferably provides a pair of spaced and opposed concentration regions in the gate oxide layer, with the area between the concentration regions being substantially undoped with chlorine and fluorine. In the context of this document, "substantially undoped" and "substantially void" means having a concentration range of less than or equal to about 1×10^{16} atoms/cm³.

Referring to Fig. 3, subsequent processing is illustrated whereby insulative sidewall spacers 36 are formed over the gate edges. A source region 38 and a drain region 40, as well as LDD regions 42, are provided.

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1 The Figs. 2-3 embodiment illustrated exemplary provision of
2 concentrated regions more proximate the gate edges by angle ion
3 implanting and subsequent anneal. Alternate processing is described
4 with other embodiments with reference to Figs. 4-10. A first alternate
5 embodiment is shown in Figs. 4-6, with like numerals from the first
6 described embodiment being utilized where appropriate, with differences
7 being indicated with the suffix "c" or with different numerals.

8 Wafer fragment 10c is shown at a processing step subsequent to
9 that depicted by Fig. 1 (however preferably with no chlorine provided
10 in the gate oxide layer). The gate oxide material of layer 16c is
11 etched substantially selective relative to silicon to remove oxide
12 thereover, as shown. A layer of oxide to be used for spacer formation
13 is thereafter deposited over substrate 12 and gate construction 18c.
14 Such is anisotropically etched to form insulative sidewall spacers 44
15 proximate opposing lateral edges 26 and 28 of gate 18. Preferably as
16 shown, such spacers are formed to cover less than all of the conductive
17 material of lateral edges 26 and 28 of gate 18. Further in this
18 depicted embodiment, such spacers 44 do not overlie any gate oxide
19 material over substrate 12, as such has been completely etched away.

20 Spacers 44 are provided to be doped with at least one of
21 chlorine or fluorine, with an example dopant concentration being
22 1×10^{21} atoms/cm³. Such doping could be provided in any of a
23 number of ways. For example, the deposited insulating layer from
24 which spacers 44 are formed, for example SiO₂, could be *in situ* doped

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1 during its formation to provide the desired fluorine and/or chlorine
2 concentration. Alternately, such could be gas diffusion doped after
3 formation of such layer, either before or after the anisotropic etch to
4 form the spacers. Further alternately, and by way of example only, ion
5 implanting could be conducted to provide a desired dopant concentration
6 within spacers 44.

7 Referring to Fig. 5, spacers 44 are annealed at a temperature and
8 for a time period effective to diffuse the dopant fluorine or chlorine
9 from such spacers into gate oxide layer 16c beneath gate 18. Sample
10 annealing conditions are as described above with respect to repair of
11 ion implantation damage. Such can be conducted as a dedicated
12 anneal, or as a byproduct of subsequent wafer processing wherein such
13 conditions are inherently provided. Such provides the illustrated
14 concentration regions 46 proximate lateral edges 26 and 28 with gate
15 oxide material therebetween preferably being substantially undoped with
16 either chlorine or fluorine.

17 Referring to Fig. 6, another layer of insulating material (i.e.,
18 silicon nitride or silicon dioxide) is deposited over gate 18 and sidewall
19 spacers 44. Such is anisotropically etched to form spacers 48 about
20 spacers 44 and gate construction 18. Preferably, such spacer 48
21 formation occurs after annealing to cause effective diffusion doping from
22 spacers 44 into gate oxide layer 16c.

23 Alternate processing with respect to Fig. 5 is shown in Fig. 7.
24 Like numerals from the first described embodiment are utilized where

appropriate with differences being indicated with the suffix "d". Here in a wafer fragment 10d, doped spacers 44 have been stripped from the substrate prior to provision of spacers 48. Accordingly, diffusion doping of chlorine or fluorine from spacers 44 would be conducted prior to such stripping in this embodiment. The Fig. 7 processing is believed to be preferred to that of Fig. 6, such that the chlorine or fluorine dopant atoms won't have any adverse effect on later or other processing steps in ultimate device operation or fabrication. For example, chlorine and fluorine may not be desired in the preferred polysilicon material of the gate.

A next alternate embodiment is described with reference to Figs. 8 and 9. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated with the suffix "e" or with different numerals. Fig. 8 illustrates a wafer fragment 10e which is similar to that depicted by Fig. 4 with the exception that gate oxide layer 16e has not been stripped or etched laterally outward of gate edges 26 and 28 prior to spacer 44e formation. Accordingly in such embodiment, spacers 44e are formed to overlie gate oxide layer 16e.

Referring to Fig. 9, such spacers are subjected to appropriate annealing conditions as described above to cause diffusion doping of the chlorine or fluorine into the gate oxide layer 16e and beneath gate 18 from laterally outward of gate edges 26 and 28. This embodiment is not believed to be as preferred as those depicted by Figs. 4-7, in that

1 the dopant must diffuse both initially downwardly into gate oxide
2 layer 16 and then laterally to beneath gate edges 26 and 28.

3 Yet another alternate embodiment is described with reference to
4 Fig. 10. Like numerals from the first described embodiment are utilized
5 where appropriate, with differences being indicated with the suffix "f".
6 Fig. 10 is similar to the Figs. 8-9 embodiment. However, gate oxide
7 layer 16f is etched only partially into laterally outward of gate edges 26
8 and 28, thus reducing its thickness. Chlorine and/or fluorine doped
9 spacers 44f are subsequently formed as described above. A diffusion
10 annealing is then conducted. In comparison to the Fig. 8 embodiment,
11 the Fig. 10 embodiment provides a portion of gate oxide layer 16f to
12 be laterally outwardly exposed, such that dopant diffusion to beneath
13 gate edges 26 and 28 is facilitated.

14 Provision of fluorine and/or chlorine at the edges, with a central
15 region therebetween being substantially void of same, reduces or
16 eliminates any adverse affect chlorine and/or fluorine would have at the
17 center of the gate where hot electron carrier effects are not as
18 prominent.

19 The above-described embodiments preferably place doped chlorine
20 or fluorine proximate both gate edges 26 and 28 within the respective
21 gate oxide layers. Alternately, such greater concentration could be
22 provided proximate only one of the gate edges, such as the drain edge
23 where the hot carrier effects are most problematic.
24

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming a transistor gate comprising:
forming a gate oxide layer over a semiconductive substrate;
providing chlorine within the gate oxide layer; and
forming a gate proximate the gate oxide layer.

2. The method of claim 1 wherein the chlorine is provided
after forming the gate.

3. The method of claim 1 wherein the chlorine is provided
before forming the gate.

4. The method of claim 1 wherein the chlorine is provided in
the gate oxide layer to a concentration of from about 1×10^{19}
atoms/cm³ to about 1×10^{21} atoms/cm³.

5. The method of claim 1 wherein the gate comprises opposing
lateral edges and a central region therebetween, the chlorine being
provided within the gate oxide layer to a greater concentration
proximate at least one of the gate edges than in the central region.

6. A method of forming a transistor gate comprising:
forming a gate and a gate oxide layer in overlapping relation, the
gate having opposing edges and a center therebetween; and
concentrating at least one of chlorine or fluorine in the gate
oxide layer within the overlap more proximate at least one of the gate
edges than the center.

7. The method of claim 6 wherein the concentrating comprises
concentrating fluorine.

8. The method of claim 6 wherein the gate is formed to have
a gate width between the edges of 0.25 micron or less, the
concentrating forming at least one concentration region in the gate oxide
which extends laterally inward from the at least one gate edge no more
than about 500 Angstroms.

9. The method of claim 6 wherein the concentrating comprises
diffusion doping.

10. The method of claim 6 wherein the concentrating comprises
ion implanting.

1 11. A method of forming a transistor gate comprising:
2 forming a gate and a gate oxide layer in overlapping relation, the
3 gate having opposing edges and a central region therebetween; and
4 doping the gate oxide layer within the overlap with at least one
5 of chlorine or fluorine proximate the opposing gate edges and leaving
6 the central region substantially undoped with chlorine and fluorine.

7
8 12. The method of claim 11 wherein the doping comprises ion
9 implanting.

10
11 13. The method of claim 11 wherein the doping provides a
12 dopant concentration in the gate oxide layer proximate the edges from
13 about 1×10^{19} atoms/cm³ to about 1×10^{21} atoms/cm³.

14
15 14. A method of forming a transistor gate comprising the
16 following sequential steps:

17 forming a gate over a gate oxide layer, the gate having opposing
18 edges; and

19 angle ion implanting at least one of chlorine or fluorine into the
20 gate oxide layer beneath the edges of the gate.

1 15. The method of claim 14 wherein the angle is between from
2 about 0.5 degrees to about 10 degrees from perpendicular the gate
3 oxide layer.

4
5 16. The method of claim 14 further comprising annealing the
6 gate oxide layer after the implanting.

7
8 17. A method of forming a transistor gate comprising the
9 following sequential steps:

10 forming a gate over a gate oxide layer, the gate having opposing
11 lateral edges; and

12 diffusion doping at least one of chlorine or fluorine into the gate
13 oxide layer beneath the gate from laterally outward of the gate edges.

14
15 18. The method of claim 17 wherein the doping provides a
16 dopant concentration in the gate oxide layer proximate the edges from
17 about 1×10^{19} atoms/cm³ to about 1×10^{21} atoms/cm³.

18
19 19. The method of claim 17 wherein the doping provides a pair
20 of spaced and opposed concentration regions in the gate oxide which
21 extend laterally inward from the gate edges no more than about
22 500 Angstroms.

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1 20. The method of claim 17 wherein the doping provides a pair
2 of spaced and opposed concentration regions in the gate oxide which
3 extend laterally inward from the gate edges no more than about
4 500 Angstroms, the concentration regions having an average dopant
5 concentration in the gate oxide layer proximate the edges from about
6 1×10^{19} atoms/cm³ to about 1×10^{21} atoms/cm³.

7
8 21. The method of claim 20 wherein the gate oxide layer
9 between the concentration regions is substantially undoped with chlorine
10 and fluorine.

11
12 22. A method of forming a transistor gate comprising the
13 following steps:

14 forming a gate over a gate oxide layer, the gate having opposing
15 lateral edges;

16 forming sidewall spacers proximate the opposing lateral edges, the
17 sidewall spacers comprising at least one of chlorine or fluorine; and

18 annealing the spacers at a temperature and for a time period
19 effective to diffuse the fluorine or chlorine from the spacers into the
20 gate oxide layer to beneath the gate.

21
22 23. The method of claim 22 wherein after the annealing,
23 stripping the spacers from the edges.

24

1 24. The method of claim 22 comprising forming the spacers to
2 cover less than all of the lateral edges.

3
4 25. The method of claim 22 comprising forming the spacers to
5 overlie the gate oxide layer.

6
7 26. The method of claim 22 comprising forming the spacers to
8 not overlie any of the gate oxide layer.

9
10 27. The method of claim 22 further comprising:
11 depositing a layer of insulating material over the gate and the
12 sidewall spacers; and
13 anisotropically etching the layer of insulating material to form
14 spacers over the sidewall spacers.

15
16 28. The method of claim 27 wherein the annealing occurs before
17 the depositing.

18
19 29. The method of claim 27 wherein the annealing occurs after
20 the depositing.

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1 30. The method of claim 22 further comprising:
2 providing gate oxide layer material laterally outward of the gate
3 edges;
4 etching only partially into the gate oxide layer laterally outward
5 of the gate edges; and
6 forming said sidewall spacers over the etched gate oxide layer
7 laterally outward of the gate edges.

8
9 31. A transistor comprising:
10 a semiconductive material and a transistor gate having gate oxide
11 positioned therebetween, the gate having opposing gate edges and a
12 central region therebetween;
13 a source formed laterally proximate one of the gate edges and a
14 drain formed laterally proximate the other of the gate edges; and
15 chlorine within the gate oxide layer between the semiconductive
16 material and the transistor gate.

17
18 32. The transistor of claim 31 wherein the chlorine is provided
19 in the gate oxide layer to a concentration of from about 1×10^{19}
20 atoms/cm³ to about 1×10^{21} atoms/cm³.

1 33. The transistor of claim 31 wherein the chlorine is provided
2 within the gate oxide layer to a greater concentration proximate at least
3 one of the gate edges than in the central region.

4
5 34. The transistor of claim 31 wherein the chlorine is provided
6 within the gate oxide layer to a greater concentration proximate the
7 other gate edge than in the central region.

8
9 35. The transistor of claim 31 wherein the chlorine is provided
10 within the gate oxide layer to a greater concentration proximate both
11 gate edges than in the central region.

12
13 36. The transistor of claim 31 wherein the central region is
14 substantially void of chlorine.

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1 37. A transistor comprising:

2 a semiconductive material and a transistor gate having gate oxide
3 positioned therebetween, the gate having opposing gate edges and a
4 central region therebetween;

5 a source formed laterally proximate one of the gate edges and a
6 drain formed laterally proximate the other of the gate edges; and

7 at least one of fluorine or chlorine being concentrated in the gate
8 oxide layer between the semiconductive material and the transistor gate
9 more proximate at least one of the gate edges than the central region.

10
11 38. The transistor of claim 37 wherein fluorine is concentrated.

12
13 39. The transistor of claim 37 wherein chlorine is concentrated.

14
15 40. The transistor of claim 37 wherein the central region of the
16 gate oxide layer is substantially void of chlorine and fluorine.

17
18 41. The transistor of claim 37 wherein the concentrated chlorine
19 or fluorine is provided in the gate oxide layer to a concentration of
20 from about 1×10^{19} atoms/cm³ to about 1×10^{21} atoms/cm³.

42. The transistor of claim 37 wherein the concentrated chlorine or fluorine is provided in the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm³ to about 1×10^{21} atoms/cm³, and wherein the central region of the gate oxide layer is substantially void of chlorine and fluorine.

43. The transistor of claim 37 wherein the at least one of fluorine or chlorine is concentrated in the gate oxide layer more proximate both gate edges than in the central region.

44. The transistor of claim 37 wherein the at least one of fluorine or chlorine is concentrated in the gate oxide layer more proximate at least the other gate edge.

45. The transistor of claim 37 wherein the gate is formed to have a gate width between the edges of 0.25 micron or less, the concentrated at least one of fluorine or chlorine extending laterally inward from the at least one gate edge no more than about 500 Angstroms.

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1 46. The transistor of claim 37 wherein the gate is formed to
2 have a gate width between the edges of 0.25 micron or less, the
3 concentrated at least one of fluorine or chlorine extending laterally
4 inward from the at least one gate edge no more than about
5 500 Angstroms with an average concentration of from about 1×10^{19}
6 atoms/cm³ to about 1×10^{21} atoms/cm³.

7
8 47. A transistor comprising:

9 a semiconductive material and a transistor gate having gate oxide
10 positioned therebetween, the gate having opposing gate edges;

11 a source formed laterally proximate one of the gate edges and a
12 drain formed laterally proximate the other of the gate edges;

13 first insulative spacers formed proximate the gate edges, the first
14 insulative spacers being doped with at least one of chlorine or fluorine;
15 and

16 second insulative spacers formed over the first insulative spacers.

17
18 48. The transistor of claim 47 wherein the second insulative
19 spacers at least as initially provided are substantially undoped with
20 either chlorine or fluorine.

1 49. The transistor of claim 47 further comprising at least one
2 of chlorine or fluorine within the gate oxide layer proximate the gate
3 edges.

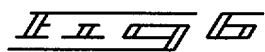
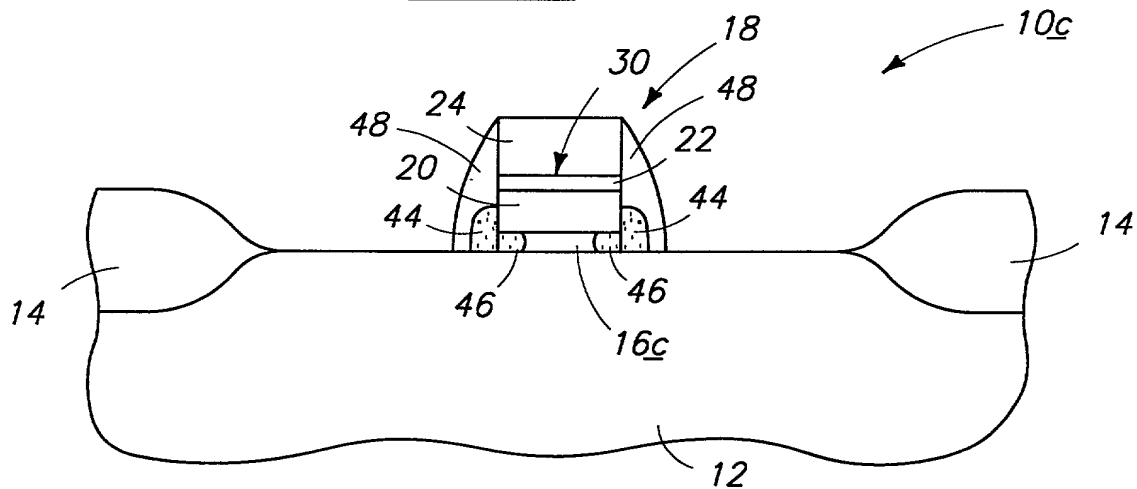
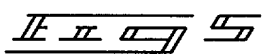
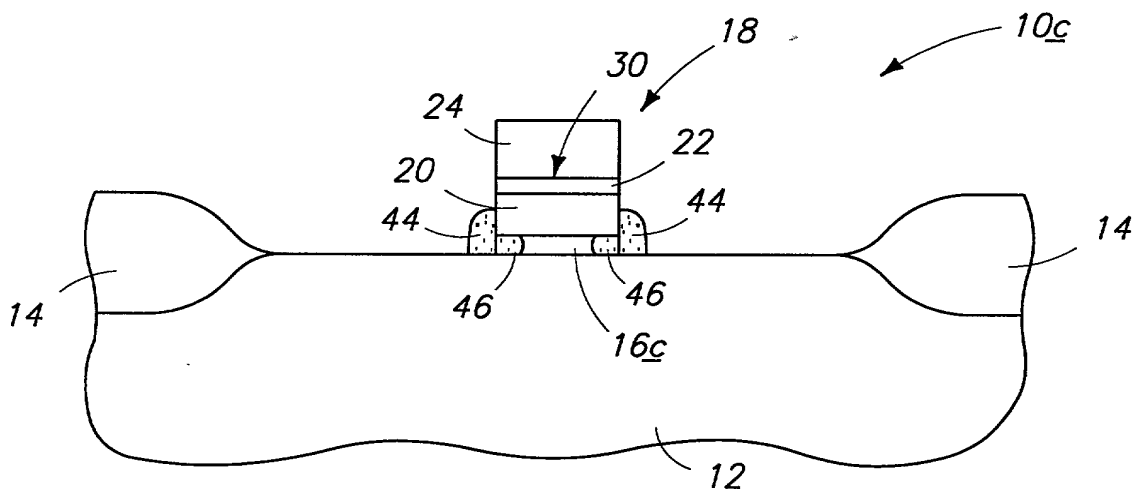
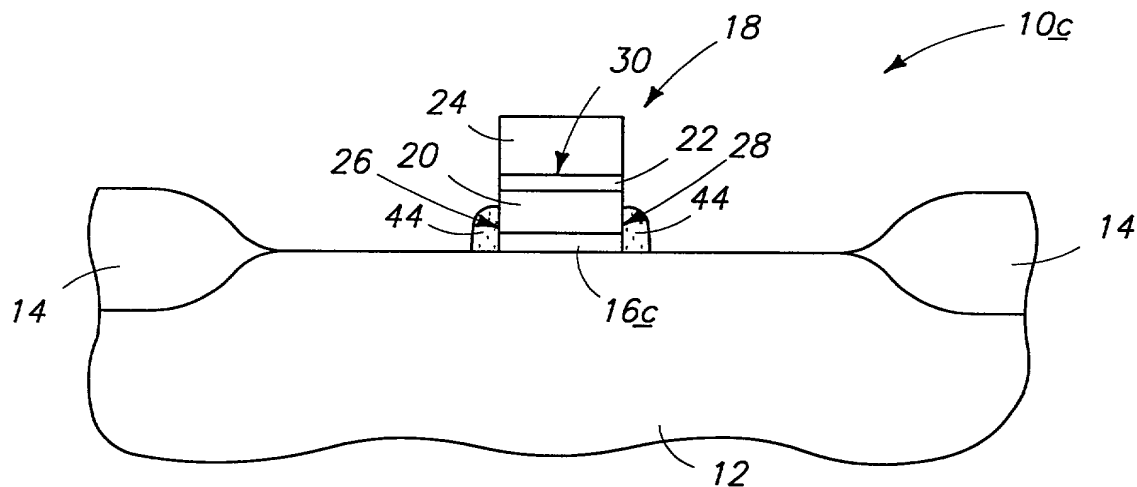
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5 50. The transistor of claim 47 wherein the gate oxide layer
6 includes a central region between the opposing gate edges, and further
7 comprising at least one of chlorine or fluorine within the gate oxide
8 layer proximate the gate edges, the central region being substantially
9 void of chlorine and fluorine.

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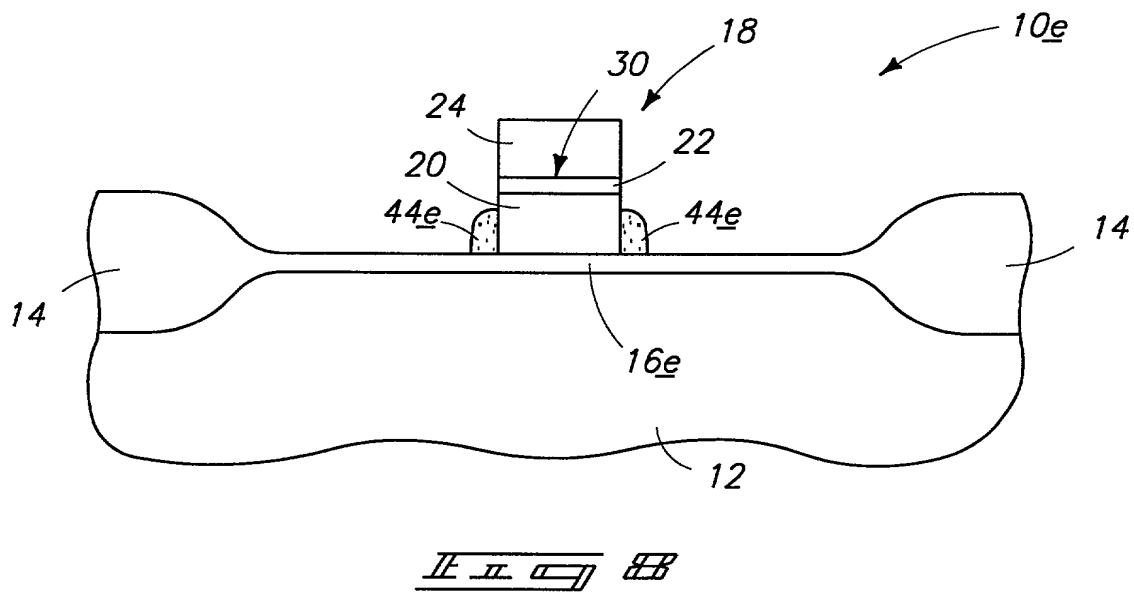
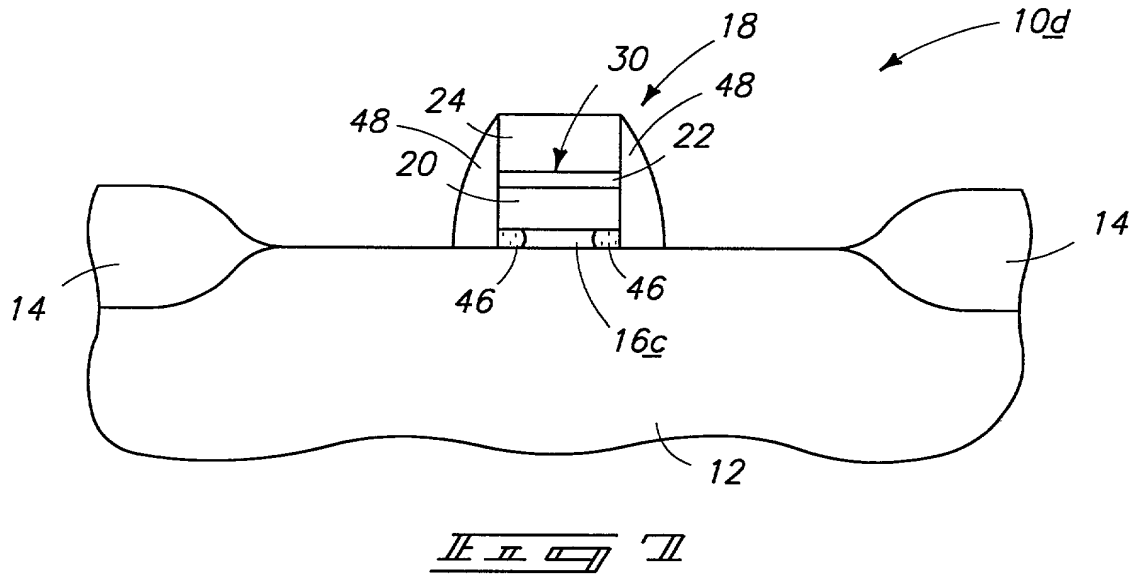
ABSTRACT OF THE DISCLOSURE

A method of forming a transistor gate includes forming a gate oxide layer over a semiconductive substrate. Chlorine is provided within the gate oxide layer. A gate is formed proximate the gate oxide layer. In another method, a gate and a gate oxide layer are formed in overlapping relation, with the gate having opposing edges and a center therebetween. At least one of chlorine or fluorine is concentrated in the gate oxide layer within the overlap more proximate at least one of the gate edges than the center. Preferably, the central region is substantially undoped with fluorine and chlorine. The chlorine and/or fluorine can be provided by forming sidewall spacers proximate the opposing lateral edges of the gate, with the sidewall spacers comprising at least one of chlorine or fluorine. The spacers are annealed at a temperature and for a time effective to diffuse the fluorine or chlorine into the gate oxide layer to beneath the gate. Transistors and transistor gates fabricated according to the above and other methods are disclosed. Further, a transistor includes a semiconductive material and a transistor gate having gate oxide positioned therebetween. A source is formed laterally proximate one of the gate edges and a drain is formed laterally proximate the other of the gate edges. First insulative spacers are formed proximate the gate edges, with the first insulative spacers being doped with at least one of chlorine or fluorine. Second insulative spacers formed over the first insulative spacers.

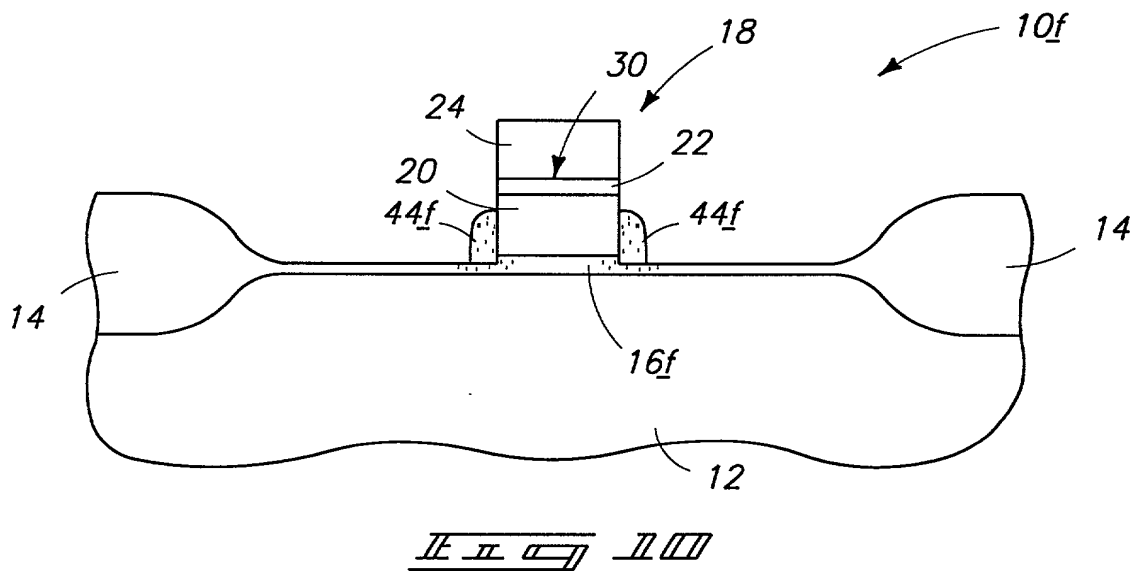
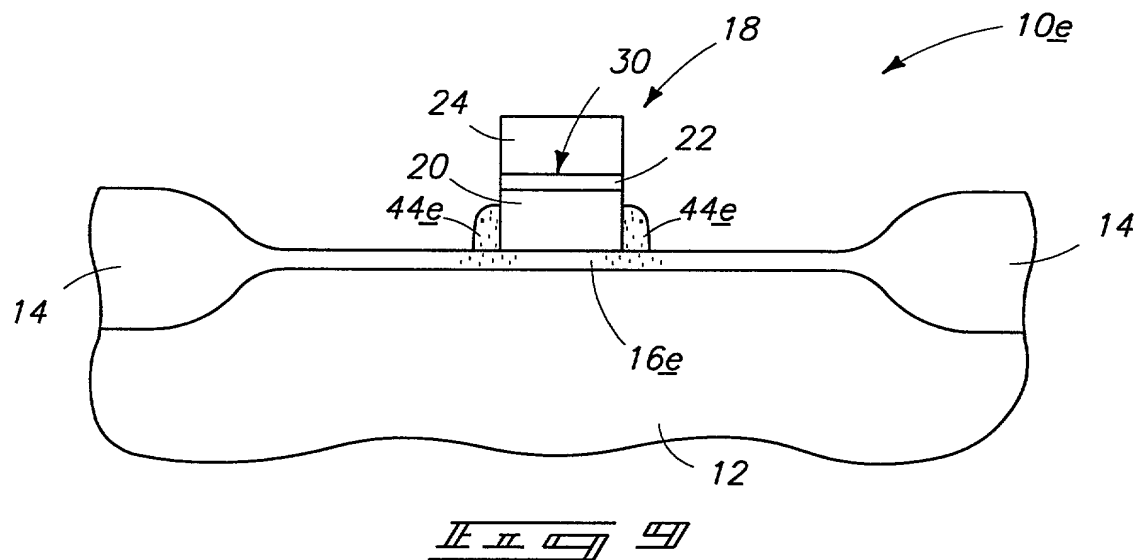
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4/4



DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Semiconductor Processing Method And Field Effect Transistor**, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

POWER OF ATTORNEY:

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10 I hereby declare that all statements made herein of my own
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15 Section 1001 of Title 18 of the United States Code and that such willful
16 false statement may jeopardize the validity of the application or any
17 patent issued therefrom.
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* * * * *

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